DESIGNING AN IMAGE SCALING PROCESSOR FOR HIGHLY ENHANCED IMAGE

Ms. L.K. Anima
Electronics and Communication Engineering
Vivekanandha College of Engineering for Women
Tiruchengode, Erode, Tamilnadu, India.

Mr.G.Yuvaraj
Electronics and Communication Engineering
Vivekanandha College of Engineering for Women
Tiruchengode, Erode,Tamilnadu, India

Abstract—This paper presents the VLSI implementation of an image scaling processor, in order to achieve low cost, high performance and low complexity. In the proposed scaling algorithm, the bilinear interpolation method is selected because of its characteristics with low complexity and high quality. The sharpening spatial and clamp filters are added as prefilters in order to reduce the blurring and aliasing artifacts produced by the bilinear interpolation. The clamp filter and sharpening spatial filters both convoluted by a 3×3 matrix coefficient kernel are combined into a 5×5 combined convolution filter which reduces the memory buffers and computing resources for the very large scale integration (VLSI) implementation. The computing resource and hardware cost of the bilinear interpolator can be efficiently reduced by an algebraic manipulation and hardware sharing techniques. A T-model and inversed T-model convolution kernels are proposed to reduce the complexity of the design. Combined filter is replaced by a dynamic estimation unit to minimize the hardware cost. Compared with previous low-complexity techniques, this work shows better performance with respect to cost and less complexity.

Keywords— Bilinear Interpolation, Clamp Filter, Image Scaling, Sharpening Spatial Filter, VLSI.

I.   INTRODUCTION

Digital image processing is a subset of the electronic domain where in the image is converted to an array of small integers, called pixels, representing a physical quantity such as scene radiance, stored in a digital memory, and processed by computer or other digital hardware. Digital image processing, either as enhancement for human observers or performing autonomous analysis, offers advantages in cost, speed, and flexibility, and with the rapidly falling price and rising performance of personal computers it has become the dominant method in use. In many applications, from consumer electronics to medical imaging, it is desirable to improve the restructured image quality and processing performance of hardware implementation. For example, a video source with a 640×480 video graphics array (VGA) resolution may need to fit the 1920×1080 resolution of a high-definition multimedia interface (HDMI). On the other hand, a high-resolution image may need to scale down to a small size in order to fit the lower resolution of small LCD panels. In recent years, a number of efficient scaling methods have been developed for image zooming. Scaling algorithm can be classified into two types as polynomial-based and non-polynomial-based.

Nearest neighbor algorithm is the uncomplicated polynomial algorithm, but resultant images are with full of aliasing artifacts. Bilinear interpolation algorithm [15] and Bi-cubic algorithm [14] are the other polynomial based methods widely used to target the pixels. For the past decade many non-polynomial high performance methods [1], [3] have been proposed. The techniques like bilateral filter [2], interpolation [1], and autoregressive model [3]. These methods are used to boost the image quality by reducing the artifacts. These Image scaling algorithms are very complex to implement in VLSI. Thus, for fast, real time applications, less complexity based algorithms are necessary [5-9]. Area pixel model Win scale method is previously proposed for less complexity methods. Adding of sharpening spatial and clamp filers effectively improves the image quality with bilinear interpolation algorithm. By these cost of the hardware and memory also reduced.

II.   PROPOSED SCALING ALGORITHM

The proposed scaling algorithm consists of a sharpening spatial filter, clamp filter and bilinear interpolation.
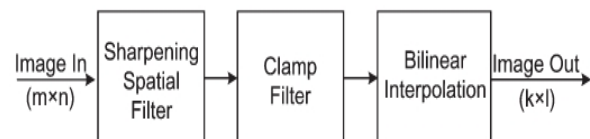
Fig 1: Block diagram of proposed scaling algorithm

Fig.1 shows the block diagram of the proposed scaling algorithm. The sharpening spatial and clamp filters [5] act as

pre- filters [4] to reduce blurring and aliasing artifacts produced by the bilinear interpolation. the input pixels of the original images are filtered by the sharpening spatial filter to enhance the edges and remove associated noise. Second, the filtered pixels are filtered again by the clamp filter to smooth unwanted discontinuous edges of the boundary regions. Finally, the pixels filtered by both of the sharpening spatial and clamp filters are passed to the bilinear interpolation for up/downscaling. To conserve computing resource and memory buffer, these two filters are simplified and combined into a combined filter.

2.1 Less complexity sharpening spatial and clamp filters

The sharpening spatial filter, a kind of high-pass filter, is used to reduce blurring artifacts and defined by a kernel to increase the intensity of a center pixel relative to its neighboring pixels. The clamp filter a kind of low pass filter is a 2-D Gaussian spatial domain filter and composed of a convolution kernel array. It usually contains a single positive value at the center and is completely surrounded by ones. The clamp filter is used to reduce aliasing artifacts and smooth the unwanted discontinuous edges of the boundary regions.

The sharpening spatial and clamp filters can be represented by convolution kernels. A larger size of convolution kernel will produce higher quality of images. However, a larger size of convolution filter will also demand more memory and hardware cost. For example, a 6×6 convolution filter demands at least a five-line-buffer memory and 36 arithmetic units, which is much more than the two-line-buffer memory and nine arithmetic units of a 3×3 convolution filter. In our previous work], each of the sharpening spatial and clamp filters was realized by a 2-D 3×3 convolution kernel. It demands at least a four-line-buffer memory for two 3×3 convolution filters. For example, if the image width is 1920 pixels, $4 \times 1920 \times 8$ bits of data should be buffered in memory as input for processing. To reduce the complexity of the 3×3 convolution kernel, a cross-model formed is used to replace the 3×3 convolution kernel. It successfully cuts down on four of nine parameters in the 3×3 convolution kernel. Furthermore, to decrease more complexity and memory requirement of the cross model convolution kernel, T-model and inversed T-model convolution kernels are proposed for realizing the sharpening spatial and clamp filters. The T-model convolution kernel is composed of the lower four parameters of the cross-model, and the inversed T-model convolution kernel is composed of the upper four parameters. In the proposed scaling algorithm, both the T-model and inversed T-model filters are used to improve the quality of the images simultaneously. The T-model or inversed T-model filter is

simplified from the 3×3 convolution filter of the previous work, which not only efficiently reduces the complexity of the convolution filter but also greatly decreases the memory requirement from two to one line buffer for each convolution filter. The T-model and the inversed T-model provide the low-complexity and low memory- requirement convolution kernels for the sharpening spatial and clamp filters to integrate the VLSI chip of the proposed low-cost image scaling processor.

2.2 Combined Filter

In proposed scaling algorithm, the input image is filtered by a sharpening spatial filter and then filtered by a clamp spatial filter again. Although the sharpening spatial and clamp filters are simplified by T-models and inversed T-models, it still needs two line buffers to store input data or intermediate values for each T-model or inversed T-model filter. Thus, to be able to reduce more computing resource and memory requirement, sharpening spatial and clamp filters, which are formed by the T-model or inversed T-model, should be combined together into a combined filter.

2.3 Bilinear interpolation

The bilinear interpolation method is selected because of its characteristics with low complexity and high quality. The bilinear interpolation is an operation that performs a linear interpolation first in one direction and, then again, in the other direction. The output pixel P (k,l) can be calculated by the operations of the linear interpolation in both x- and y-directions with the four nearest neighbor pixels. We can easily find that the computing resources of the bilinear interpolation cost eight multiply, four subtract, and three addition operations. It costs a considerable chip area to implement a bilinear interpolator with eight multipliers and seven adders. Thus, an algebraic manipulation skill has been used to reduce the computing resources of the bilinear interpolation.

III.   VLSI ARCHITECTURE

The proposed scaling algorithm consists of two combined pre-filters and one simplified bilinear interpolator.For VLSI implementation, the bilinear interpolator can directly obtain two input pixels.The proposed scaling algorithm consists of two combined pre-filters and one simplified bilinear interpolator.For VLSI implementation, the bilinear interpolator can directly obtain two input pixels.

3.1 Register Bank
In this brief, the combined filter is filtering to produce the target pixels of P(m,n) and P(m,n+1) by using ten source pixels.
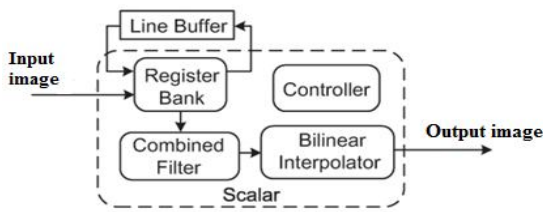
Corresponding Author: Ms. L.K. Anima, Vivekanandha College of Engineering and Technology for Women, Tamilnadu , India.   184

Fig 2: VLSI architecture for proposed real-time image scaling processor

The register bank is designed with a one-line memory buffer, which is used to provide the ten values for the immediate usage of the combined filter. Fig. 3 shows the architecture of the register bank with a structure of ten shift registers.
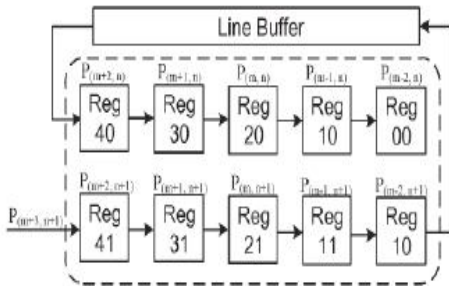

Fig 3: Architecture of the register bank

When the shifting control signal is produced from the controller, a new value of P(m+3,n) will be read intoReg41, and each value stored in other registers belonging to row $n + 1$ will be shifted right into the next register or line-buffer memory. The Reg40 reads a new value of P(m+2,n) from the line-buffer memory, and each value in other registers belonging to row n will be shifted right into the next register.

3.2 Combined Filter

The combined T-model or inversed T-model convolution function of the sharpening spatial and clamp filters. Fig. 4 shows the six-stage pipelined architecture of the combined filter and bilinear interpolator, which shortens the delay path to improve the performance by pipeline technology. The stages 1 and 2 in Fig. 4 show the computational scheduling of a T-model combined and an inverse T-model filter. The T-model or inversed T-model filter consists of three reconfigurable calculation units (RCUs), one multiplier–adder (MA), three adders (+), three subtracters (−), and three shifters (S). The hardware architecture of the T-model combined filter can be directly mapped with the convolution equation shown in (1). The values of the ten source pixels can be obtained from the register bank mentioned earlier.
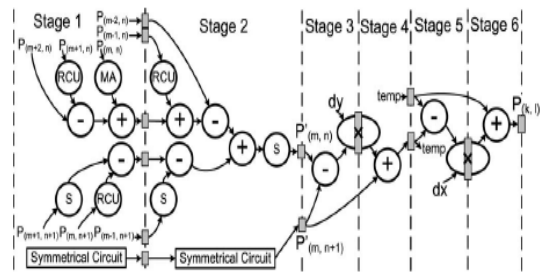

Fig 4: Computational scheduling of the proposed combined filter and simplified bilinear interpolator

The symmetrical circuit, as shown in stages 1 and 2 of Fig.3, is the inversed T-model combined filter designed for producing the filtered result of p (m, n+1). Obviously, The T-model and the inversed T-model are used to obtain the values of p (m, n) and p (m, n + 1) simultaneously. The architecture of this symmetrical circuit is a similar symmetrical structure of the T-model combined filter, as shown in stages 1 and 2 of Fig. 3. Both of the combined filter and symmetrical circuit consist of one MA and three RCUs. The MA can be implemented by a multiplier and an Adder. The RCU is designed for producing the calculation functions of (S-C) and (S-C-1) times of the source pixel value, which must be implemented with C and S parameters. The C and S parameters can be set by users according to the characteristics of the images
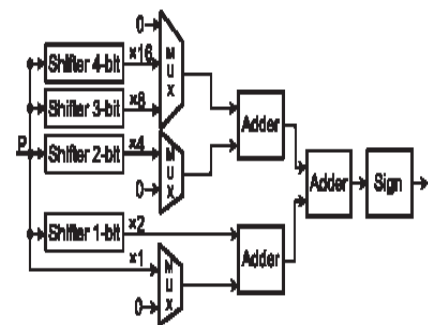

Fig 5 : Architecture of the RCU

Fig. 5 shows the architecture of the RCU. It consists of four shifters, three multiplexers (MUX), three adders, and one sign circuit. By this RCU design, the hardware cost of the combined filters can be efficiently reduced.

3.3 Bilinear Interpolator and Controller

The bilinear interpolation is simplified as shown in (5). The stages 3, 4, 5, and 6 in Fig. 4 show the four-stage pipelined

architecture, and two-stage pipelined multipliers are used to shorten the delay path of the bilinear interpolator. The input values of   P (m, n) and P (m,n+1) are obtained from the combined filter and symmetrical circuit. By the hardware sharing technique, as shown in (4), the temperature result of the function "P (m, n) + dy × (P (m,n+1) − P (m, n))" can be replaced by the previous result of "P(m+1,n) + dy × (P(m+1,n+1)− P(m+1i,n))." It also means that one multiplier and two adders can be successfully reduced by adding only one register. The controller is implemented by a finite-state machine circuit. It produces control signals to control the timing and pipeline stages of the register bank, combined filter, and bilinear interpolator.

Fig 8: HDL simulation

IV.   SIMULATION RESULTS

Here *cameraman.tif* is used as a noisy input image. The MATLAB and HDL simulation results are given by

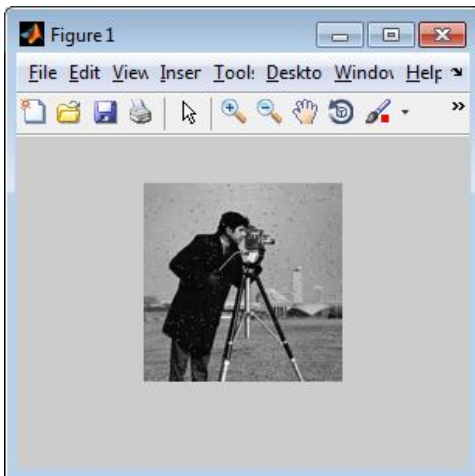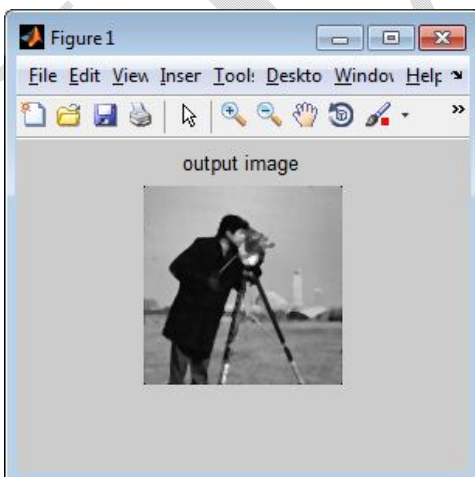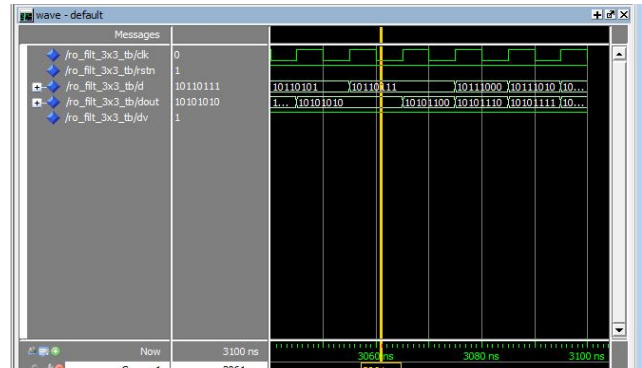*Fig 6 : Noisy input image*

Fig 7 : Enhanced output image

V.   CONCLUSION

A novel adaptive scaling algorithm is proposed for developing a low-cost, low-complexity and high quality VLSI scaling circuit for image zooming applications. Bilinear interpolation is selected as an interpolation method due to its low complexity and high quality. A clamp filter and a sharpening spatial filter are added as pre-filters to solve the shortcomings of blurring and aliasing effects caused by the bilinear interpolation. With added adaptive skill, the quality of the resulting scaled images is notably improved. Techniques of filter combination, co-operation, and hardware sharing greatly reduce memory buffer requirements and hardware costs. Relative to previous low-complexity VLSI scalar designs,this work achieves reduction in gate counts and requires only one-line memory buffer

References

[1]   H. Kim, Y. Cha, and S. Kim, "Curvature interpolation method for image zooming," IEEE Trans. Image Process.,vol. 20, no. 7, pp. 1895–1903, Jul. 2011.

[2]   J. W. Han, J. H. Kim, S. H. Cheon, J.O.Kim, and S. J. Ko, "Anovel Image interpolation method using the bilateralfilter," IEEE Trans. Consum.Electron., vol. 56, no. 1, pp. 175–181, Feb. 2010

[3]   X. Zhang and X.Wu, "Image interpolation by adaptive 2-D autoregressive modeling and soft-decision estimation,"IEEE Trans Image Process., vo17, no. 6, pp. 887–896, Jun. 2008.

[4]   F. Cardells-Tormo and J. Arnabat-Benedicto, "Flexible hardware Friendly digital architecture for 2-D separable convolution-based scaling," IEEE Tran, Exp. Briefs, vol. 53, no. 7, pp. , Jul. 2006.

[5]   S. Ridella, S. Rovetta, and R. Zunino, "IAVQ-interval-arithmetic vector quantization for image compression," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, pp. 1378–1390, Dec. 2000.

[6]   S. Saponara, L. Fanucci, S. Marsi, G. Ramponi, D. Kammler, and E. M. Witte, "Application-specific instruction-set processor for Retinexlink image and video processing," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 7, pp.596–600, Jul. 2007.

[7]   P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," IEEE Tran, Exp. Briefs, vol. 56, no. 1, pp. 51–55, Jan. 2009.

[8]   M. Fons, F. Fons, and E. Canto, "Fingerprint image processing acceleration through run-time reconfigurable hardware," IEEE Trans. Circuits Syst. II, Exp., vol. 57, no. 12, pp. 991–995, Dec. 2010.

[9]   C. H. Kim, S. M. Seong, J. A. Lee, and L. S. Kim, "Winscale : An imagescaling algorithm using an area pixelmodel," IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 6, pp. 549–553, Jun. 2003.

[10] C. C. Lin, Z. C. Wu, W. K. Tsai, M. H. Sheu, and H. K. Chiang, "The VLSI design of winscale for digital image scaling," in Proc. IEEEInt. Conf. Intell. Inf. Hiding Multimedia Signal Process., Nov. 2007, pp 511–514

[11] P. Y. Chen, C. Y. Lien, and C. P. Lu, "VLSI implementation of an edgeoriented image scaling processor," IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 17, no. 9, pp. 1275–1284, Sep. 2009.

[12] C. C. Lin, M. H. Sheu, H. K. Chiang, W. K. Tsai, and Z. C. Wu, "Real-time FPGA architecture of extended linear convolution for digital image scaling," in Proc. IEEE Int. Conf. Field-Program. Technol., 2008, pp. 381–384.

[13] C. C. Lin, M. H. Sheu, H. K. Chiang, C. Liaw, and Z. C. Wu, "The efficient VLSI design of BI-CUBIC convolution interpolation for digital image processing," in Proc. IEEE Int Conf. Circuits Syst., May 2008. pp. 480–483.

[14] S. L. Chen, H. Y. Huang, and C. H. Luo, "A low-cost high-quality adaptive scalar for real-time multimedia applications," IEEE Trans. Circuits Syst.Video Technol., vol. 21, no. 11, pp. 1600–1611, Nov. 2011.

[15] K. Jensen and D. Anastassiou, "Subpixel edge localization and the interpolation of still images," IEEE Trans. ImageProcess., vol. 4, no. 3, pp. 285–295, Mar. 1995.